Factsheet

UART eVC – SI71U*e*VC10

Silicon Cores™

Core to the Intelligent System™

*e*VC UART

Silicon Interfaces' UART *e*VC is a fully documented, off the shelf component for Cadence Specman Elite™ functional verification environment. At the heart of every asynchronous serial system is the Universal Asynchronous Receiver/Transmitter (UART). The UART is responsible for implementing the asynchronous communication process as both a transmitter and a receiver (both encoding and decoding data frames). The UART not only controls the transfer of data, but the speed at which communication takes place.

The UART *e*VC is designed to have generation of data bits and testing of output data according to protocol. It also generates and tests data for error condition and corner cases also. It handles all the three modes: FIFO mode, Auto flow mode and Loop-back mode.

*e*VCs are configurable, reusable verification components written in the *e* language and designed to simplify and speed up the verification tasks. These comprise a complete verification environment including stimulus generation, checking, monitoring and functional coverage. *e*VCs provide major increase in the productivity and higher quality products.

The UART eVC exhaustively tests the databus control mechanism, interrupt logic, command and status registers, FIFO, transmitter, receiver, baud-rate generator, modem control interface. The UART *e*VC verifies designs that include UART. This *e*VC accurately verifies and ensures that the particular UART is satisfying the protocol. It includes number of start bits per character, number of stop bits per character, parity and break control. Verifying the baud rate generator module is crucial. This VIP thoroughly checks the half-divisor value and full divisor value loaded in divisor latches in the UART.

Product Highlights

- ☑ Fully compliant with the UART specifications.
- ☑ Supports transmission interface on one side & reception on other side.
- ☑ Protocol Compliance checking.
- ☑ Generates the stimulus compliant to transmission interface and reception interface.
- ☑ Provides monitoring of signals and data in transmit and receive directions.
- ☑ Provides stop bits error notification.
- ☑ Provides parity error notification.
- ☑ Provides break error notification.
- ☑ Provides monitoring of signals and timings for reset, FIFO, Autoflow and Loopback mode
- ☑ Generates different number of bits per character and checks for it.
- ☑ Generates different number of stop bits and checks for it
- ☑ Generates odd, even and no parity and checks for it.
- ☑ Provides the coverage information
- ☑ HDL independent.

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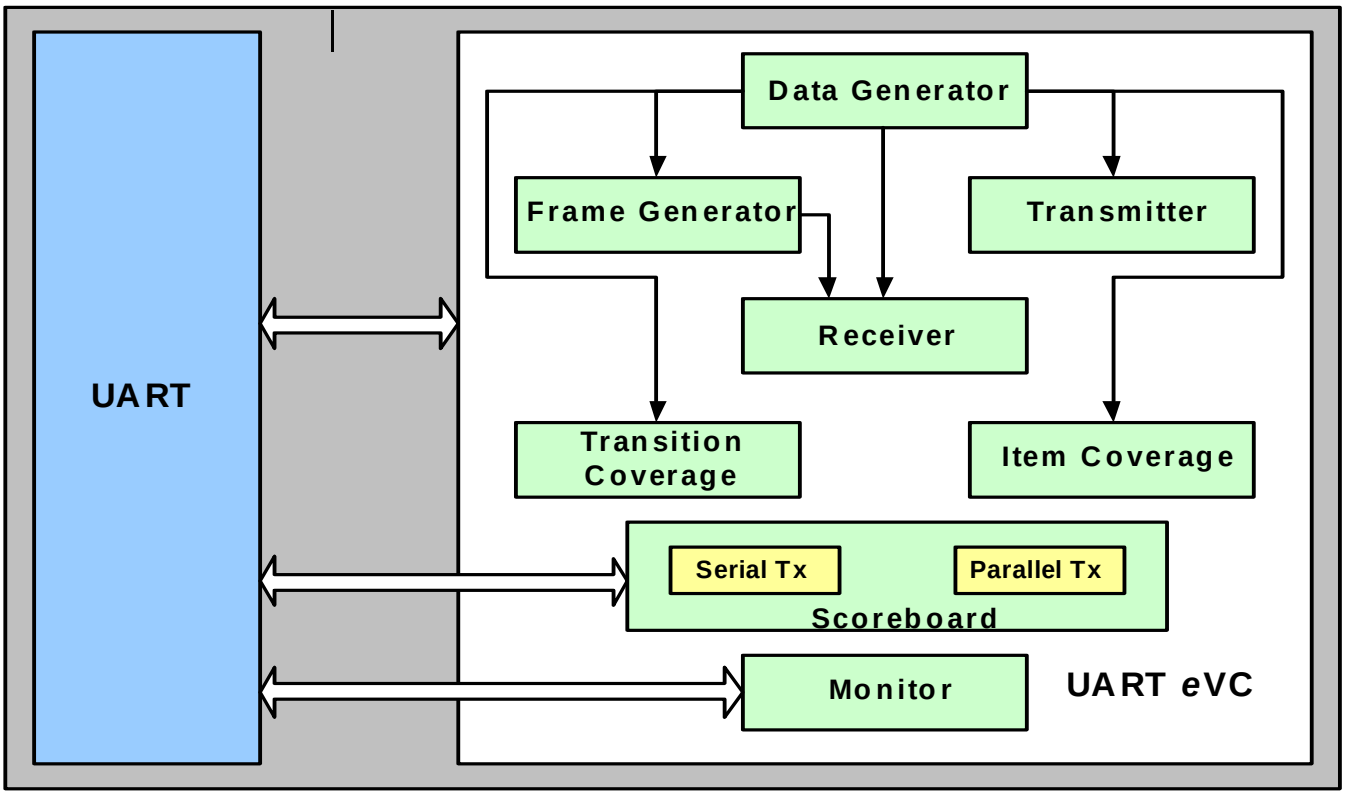
Modules of UART eVC

UART eVC contains 9 modules.

1) Data Generator : Defines the strecture of 12 registers.
2) Data Driver : Drives the data to the DUT.
3) Frame Generator : Defines the fields in the frame.
4) Receiver-Driver : Drives the serial data to the SIN (Serial Input) pin with all the considerations of start bit, stop bit, no.of bits/character, parity enable, parity.
5) Coverage : It does the coverage of all the statemachines in the UART modules.
6) Icoverage : It does the coverage of all the fields used in eVC data generator.
7) Serial-rx : It works as a scoreboard.
8) Parallel-rx : Works as a scoreboard.
9) Monitor : Checks for timing of UART.

UART Block Representative Schematic:



Verification Methodology:

An *e*VC applies parallel data to UART DUT according to protocol in transmission mode. In receiver mode it applies serial data according to protocol. At all the times the *e*VC Monitor monitors the timing issues during transmission & reception. The captured data is checked by the *e*VC checker to verify the adherence to the UART mode and protocol.

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